

Date: December 18,1998 Rev Date: December 18, 1998

**Project:** CFT/CPS/FPS **Doc. No:** A981218A

**Subject:** Guidelines for specifying charge division components

#### Introduction

The SIFT circuit in the CFT, CPS and FPS systems requires a charge division network at the input in order to work correctly. Various values of capacitors are used in order to scale the gain of the SIFT discriminator to the detector element involved. The network has limits on various component values which are discussed below. In addition, capacitive elements must have sufficient frequency response, which limits the selection based upon dielectric type.

#### Circuit Network

A generic drawing of the SIFT input network (SPICE model) is shown in Figure 1.

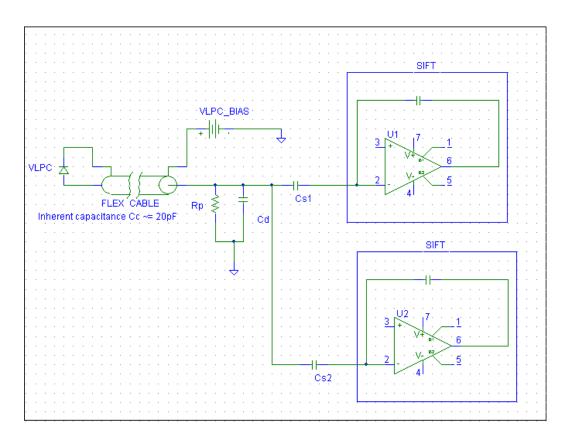


Figure 1

The charge generated by the VLPC goes through the Flex Cable (and is affected by Cc), shunts through Rp and Cd to ground, but some goes into the SIFT channels through Cs1 and Cs2. Various relationships affect the boundary values of these components.

# **Boundary Conditions**

#### **VLPC Bias Current**

The VLPC has a standing bias current of approximately 1 uA. This DC current flows through Rp and generates a DC offset voltage which affects the actual voltage dropped across the VLPC. If Rp is greater than 100 K ohms, the voltage across Rp will be greater than 0.1 volt. Variances from VLPC to VLPC would then result in too much bias voltage differential between VLPCs, generating unacceptable gain variations.

### Measurement Accuracy during Acquisition Window

The SIFT has a charge acquisition window of 50 to 70 nsec. The discharge time constant  $T_{\rm disc}$  formed by Rp and (Cc + Cd) must be long with respect to that time (say, 1 usec) in order to insure that the charge stays in the SIFT during the acquisition time. The transfer time constant  $T_{\rm xfr}$  of Cs \* 600 (the time constant associated with the charge entering the SIFT, using a nominal input impedance of 600 ohms), should be short with respect to 50-70 nsec, say about 1-2 nsec.

# Input Impedance of SIFT

The input impedance of the SIFT is estimated to be about 600 ohms at 200 MHz. Ideally, the reactance of Cs should be as large as possible so that the offset voltage generated by that input impedance is minimized. This means that Cs should be as small as practically possible.

## Accuracy of Division Ratio

The flex cable inherent capacitance Cc is not well known and the amount of variation from cable to cable is also not well known. Therefore, Cd should be as large as possible to minimize variance in the charge division ratio between channels in a cable, and from cable to cable. The estimated value of Cc, used throughout this document, is 25 pF.

## Consistency of capacitance seen by SIFT input

The series combination of Cs and (Cc + Cd) should be kept reasonably constant across channels in a board to insure all channels see the same noise voltage. The formula

$$Cnet = \frac{(Cd + Cc) * Cs}{Cd + Cc + Cs} \le 33 \, pF$$

should be observed to insure minimum noise.

#### Minimization of Crosstalk

Cs1 & Cs2 should be as small as possible to minimize crosstalk between the two SIFT channels.

# Working out some desired ratios

- 1. Say the desired ratio of Cs to (Cd+Cc) is 1/10.
  - In this scenario, we set Rp to 100 K ohms (maximal value).
  - To obtain a T<sub>disc</sub> of >1 usec, (Cd + Cc) must be greater than 10 pF. Since Cc is already 25 pF, no problem.
  - To minimize cable variation errors, Cd is arbitrarily set to 50 pF.
  - With a ratio of 1/10, Cs is therefore 7.5 pF.
  - This results in a  $T_{xfr}$  of 4.6 nsec.
  - The chosen capacitor values yield a C<sub>net</sub> of 6.8 pF.

- 2. Say the desired ratio of Cs to (Cd + Cc) is 1/3.
  - In this scenario, we set Rp to 100 K ohms (maximal value).
  - To obtain a T<sub>disc</sub> of >1 usec, (Cd + Cc) must be greater than 10 pF. Since Cc is already 25 pF, no problem.
  - To minimize cable variation errors, Cd is arbitrarily set to 50 pF.
  - With a ratio of 1/3, Cs is therefore 25 pF.
  - This results in a  $T_{xfr}$  of 15 nsec. This is probably too long and measurement errors will result.
  - To compensate, Cs could be scaled back to 8 pF; this would then require Cd to be zero, which results in errors due to cable variation.
  - The net result is that a ratio of 1/3 is too small and should be avoided.

#### **Conclusions**

Given the various constraints, the ratio of Cs to (Cd + Cc) should be kept to no more than 20%, or 1/5, and ideally, no more than 10% (1/10).